40-Channel, 14-Bit, Serial Input, Voltage Output DAC

AD5371

FEATURES

- 40-channel DAC in 80-lead LQFP and 100-ball CSP_BGA
- Guaranteed monotonic to 14 bits
- Maximum output voltage span of 4 × V_{REF} (20 V)
- Nominal output voltage span of −4 V to +8 V
- Multiple, independent output voltage spans available
- System calibration function allowing user-programmable offset and gain
- Channel grouping and addressing features
- Thermal shutdown function
- DSP/microcontroller-compatible serial interface
- SPI/LVDS serial interface
- 2.5 V to 5.5 V digital interface
- Digital reset (RESET)
- Clear function to user-defined SIGGNDx
- Simultaneous update of DAC outputs

APPLICATIONS

- Level setting in automatic test equipment (ATE)
- Variable optical attenuators (VOA)
- Optical switches
- Industrial control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

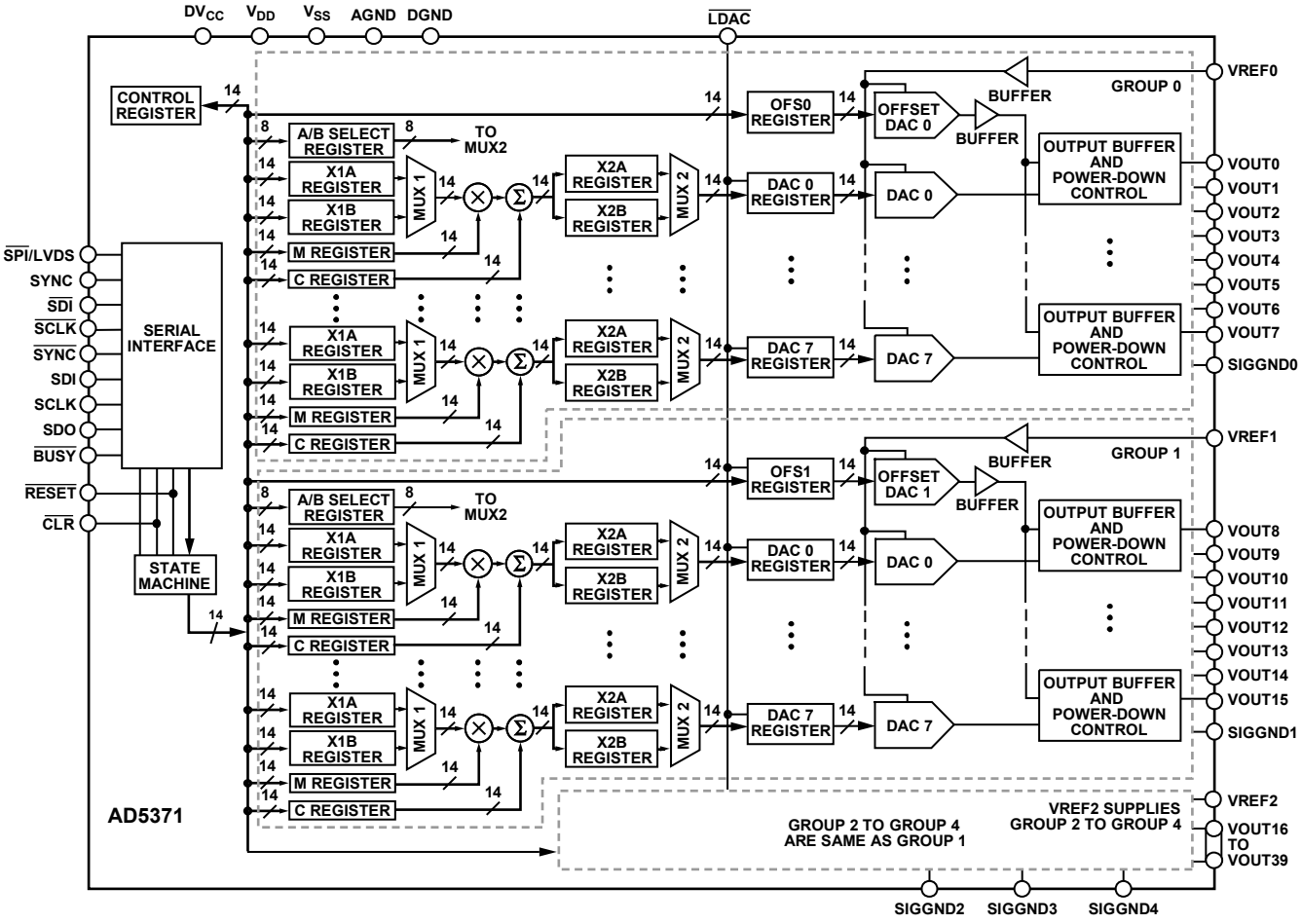

Figure 1.

Rev. B

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8/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5371[1] contains 40 14-bit DACs in a single 80-lead LQFP or 100-ball CSP_BGA. The device provides buffered voltage outputs with a span of 4× the reference voltage. The gain and offset of each DAC can be independently trimmed to remove errors. For even greater flexibility, the device is divided into five groups of eight DACs. Three offset DACs allow the output range of the groups to be adjusted. Group 0 can be adjusted by Offset DAC 0, Group 1 can be adjusted by Offset DAC 1, and Group 2 to Group 4 can be adjusted by Offset DAC 2.

The AD5371 offers guaranteed operation over a wide supply range, with V_{SS} from −16.5 V to −4.5 V and V_{DD} from 9 V to 16.5 V. The output amplifier headroom requirement is 1.4 V operating with a load current of 1 mA.

[1] Protected by U.S. Patent No. 5,969,657; other patents pending.

The AD5371 has a high speed serial interface that is compatible with SPI, QSPI™, MICROWIRE™, and DSP interface standards and can handle clock speeds of up to 50 MHz. It also has a 100 MHz low voltage differential signaling (LVDS) serial interface.

The DAC registers are updated on reception of new data. All the outputs can be updated simultaneously by taking the $\overline{\text{LDAC}}$ input low. Each channel has a programmable gain and an offset adjust register to allow removal of gain and offset errors.

Each DAC output is gained and buffered on chip with respect to an external SIGGNDx input. The DAC outputs can also be switched to SIGGNDx via the $\overline{\text{CLR}}$ pin.

Table 1. High Channel Count Bipolar DACs

Model	Resolution (Bits)	Nominal Output Span	Output Channels	Linearity Error (LSB)
AD5360	16	$4 \times V_{REF}$ (20 V)	16	±4
AD5361	14	$4 \times V_{REF}$ (20 V)	16	±1
AD5362	16	$4 \times V_{REF}$ (20 V)	8	±4
AD5363	14	$4 \times V_{REF}$ (20 V)	8	±1
AD5370	16	$4 \times V_{REF}$ (12 V)	40	±4
AD5371	14	$4 \times V_{REF}$ (12 V)	40	±1
AD5372	16	$4 \times V_{REF}$ (12 V)	32	±4
AD5373	14	$4 \times V_{REF}$ (12 V)	32	±1
AD5378	14	±8.75 V	32	±3
AD5379	14	±8.75 V	40	±3

SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

DV_{CC} = 2.5 V to 5.5 V; V_{DD} = 9 V to 16.5 V; V_{SS} = −16.5 V to −8 V; VREF = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = open circuit; R_L = open circuit; gain (M), offset (C), and DAC offset registers at default values; temperature range for the AD5371 is −40°C to +85°C; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments[1]
ACCURACY					
Resolution		14		Bits	
Integral Nonlinearity (INL)	−1		+1	LSB	
Differential Nonlinearity (DNL)	−1		+1	LSB	Guaranteed monotonic by design
Zero-Scale Error	−10		+10	mV	Before calibration
Full-Scale Error	−10		+10	mV	Before calibration
Gain Error			0.1	% FSR	
Zero-Scale Error[2]		1		LSB	After calibration
Full-Scale Error[2]		1		LSB	After calibration
Span Error of Offset DAC	−35		+35	mV	See the Offset DACs section for details
VOUTx Temperature Coefficient (VOUT0 to VOUT39)		5		ppm FSR/°C	Includes linearity, offset, and gain drift
DC Crosstalk[2]			120	µV	Typically 20 µV; measured channel at midscale, full-scale change on any other channel
REFERENCE INPUTS (VREF0, VREF1, VREF2)[2]					
VREFx Input Current	−10		+10	µA	Per input; typically ±30 nA
VREFx Range	2		5	V	±2% for specified operation
SIGGND INPUTS (SIGGND0 TO SIGGND4)[2]					
DC Input Impedance	50			kΩ	Typically 55 kΩ
Input Range	−0.5		+0.5	V	
SIGGNDx Gain	0.995		1.005		
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range	V_{SS} + 1.4		V_{DD} − 1.4	V	I_{LOAD} = 1 mA
Nominal Output Voltage Range	−4		+8	V	
Short-Circuit Current			15	mA	VOUTx to DV_{CC}, V_{DD}, or V_{SS}
Load Current	−1		+1	mA	
Capacitive Load			2200	pF	
DC Output Impedance			0.5	Ω	
DIGITAL INPUTS					
Input High Voltage	1.7			V	DV_{CC} = 2.5 V to 3.6 V
	2.0			V	DV_{CC} = 3.6 V to 5.5 V
Input Low Voltage			0.8	V	DV_{CC} = 2.5 V to 5.5 V
Input Current	−1		+1	µA	Excluding $\overline{CLR}$ pin
$\overline{CLR}$ High Impedance Leakage Current	−20		+20	µA	
Input Capacitance[2]			10	pF	
DIGITAL OUTPUTS (SDO, $\overline{BUSY}$)					
Output Low Voltage			0.5	V	Sinking 200 µA
Output High Voltage (SDO)	DV_{CC} − 0.5			V	Sourcing 200 µA
SDO High Impedance Leakage Current	−5		+5	µA	
High Impedance Output Capacitance[2]		10		pF	

Parameter	Min	Typ[1]	Max	Unit	Test Conditions/Comments[1]
LVDS INTERFACE (REDUCED RANGE LINK)					
Digital Inputs[2]					
Input Voltage Range	875		1575	mV	
Input Differential Threshold	−0.1		+0.1	V	
External Termination Resistance	80	100	132	Ω	
Differential Input Voltage	100			mV	
POWER REQUIREMENTS					
DV_{CC}	2.5		5.5	V	
V_{DD}	9		16.5	V	
V_{SS}	−16.5		−4.5	V	
Power Supply Sensitivity[2]					
ΔFull Scale/ΔV_{DD}		−75		dB	
ΔFull Scale/ΔV_{SS}		−75		dB	
ΔFull Scale/ΔDV_{CC}		−90		dB	
DI_{CC}			2	mA	DV_{CC} = 5.5 V, V_{IH} = DV_{CC}, V_{IL} = GND; normal operating conditions
I_{DD}			18	mA	Outputs unloaded, DAC outputs = 0 V
			20	mA	Outputs unloaded, DAC outputs = full scale
I_{SS}			−18	mA	Outputs unloaded, DAC outputs = 0 V
			−20	mA	Outputs unloaded, DAC outputs = full scale
Power Dissipation Unloaded (P)		280		mW	V_{SS} = −8 V, V_{DD} = 9.5 V, DV_{CC} = 2.5 V
Power-Down Mode					Control register power-down bit set
DI_{CC}		5		µA	
I_{DD}		35		µA	
I_{SS}		−35		µA	
Junction Temperature[3]			130	°C	$T_J = T_A + P_{TOTAL} \times \theta_{JA}$

[1] Typical specifications are at 25°C.
[2] Guaranteed by design and characterization; not production tested.
[3] θ_{JA} represents the package thermal impedance.

AC CHARACTERISTICS

DV_{CC} = 2.5 V; V_{DD} = 15 V; V_{SS} = −15 V; VREF = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = 200 pF; R_L = 10 kΩ; gain (M), offset (C), and DAC offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3. AC Characteristics[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time		20		µs	Settling to 1 LSB from a full-scale change
			30	µs	DAC latch contents alternately loaded with all 0s and all 1s
Slew Rate		1		V/µs	
Digital-to-Analog Glitch Energy		5		nV-s	
Glitch Impulse Peak Amplitude			10	mV	
Channel-to-Channel Isolation		100		dB	VREF0, VREF1, VREF2 = 2 V p-p, 1 kHz
DAC-to-DAC Crosstalk		20		nV-s	
Digital Crosstalk		0.2		nV-s	
Digital Feedthrough		0.02		nV-s	Effect of input bus activity on DAC output under test
Output Noise Spectral Density @ 10 kHz		250		nV/√Hz	V_{REF} = 0 V

[1] Guaranteed by design and characterization; not production tested.

TIMING CHARACTERISTICS

DV_{CC} = 2.5 V to 5.5 V; V_{DD} = 9 V to 16.5 V; V_{SS} = −16.5 V to −8 V; VREFx = 3 V; AGND = DGND = SIGGNDx = 0 V; C_L = 200 pF to GND; R_L = open circuit; gain (M), offset (C), and DAC offset registers at default values; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4. SPI Interface

Parameter [1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	20	ns min	SCLK cycle time
t_2	8	ns min	SCLK high time
t_3	8	ns min	SCLK low time
t_4	11	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	20	ns min	Minimum $\overline{SYNC}$ high time
t_6	10	ns min	24th SCLK falling edge to $\overline{SYNC}$ rising edge
t_7	5	ns min	Data setup time
t_8	5	ns min	Data hold time
t_9 [4]	42	ns max	$\overline{SYNC}$ rising edge to $\overline{BUSY}$ falling edge
t_{10}	1/1.5	µs typ/µs max	$\overline{BUSY}$ pulse width low (single-channel update); see Table 9
t_{11}	600	ns max	Single-channel update cycle time
t_{12}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{13}	10	ns min	$\overline{LDAC}$ pulse width low
t_{14}	3	µs max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	3	µs max	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	20/30	µs typ/µs max	DAC output settling time
t_{18}	140	ns max	$\overline{CLR}$/$\overline{RESET}$ pulse activation time
t_{19}	30	ns min	$\overline{RESET}$ pulse width low
t_{20}	400	µs max	$\overline{RESET}$ time indicated by $\overline{BUSY}$ low
t_{21}	270	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_{22} [5]	25	ns max	SCLK rising edge to SDO valid
t_{23}	80	ns max	$\overline{RESET}$ rising edge to $\overline{BUSY}$ falling edge

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 4 and Figure 5.
[4] t_9 is measured with the load circuit shown in Figure 2.
[5] t_{22} is measured with the load circuit shown in Figure 3.

Table 5. LVDS Interface

Parameter [1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	12	ns min	SCLK cycle time
t_2	5	ns min	SCLK pulse width high and low time
t_3	5	ns min	$\overline{SYNC}$ to SCLK setup time
t_4	3	ns min	Data setup time
t_5	3	ns min	Data hold time
t_6	3	ns min	SCLK to $\overline{SYNC}$ hold time
t_7	10	ns min	$\overline{SYNC}$ high time

[1] Guaranteed by design and characterization; not production tested.
[2] All input signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 6.

Circuit and Timing Diagrams

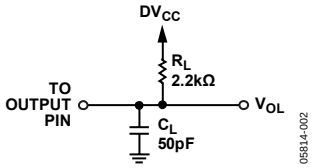


Figure 2. Load Circuit for $\overline{BUSY}$ Timing Diagram

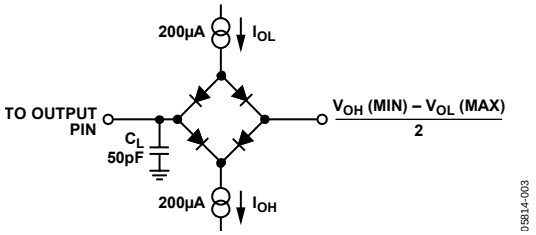


Figure 3. Load Circuit for SDO Timing Diagram

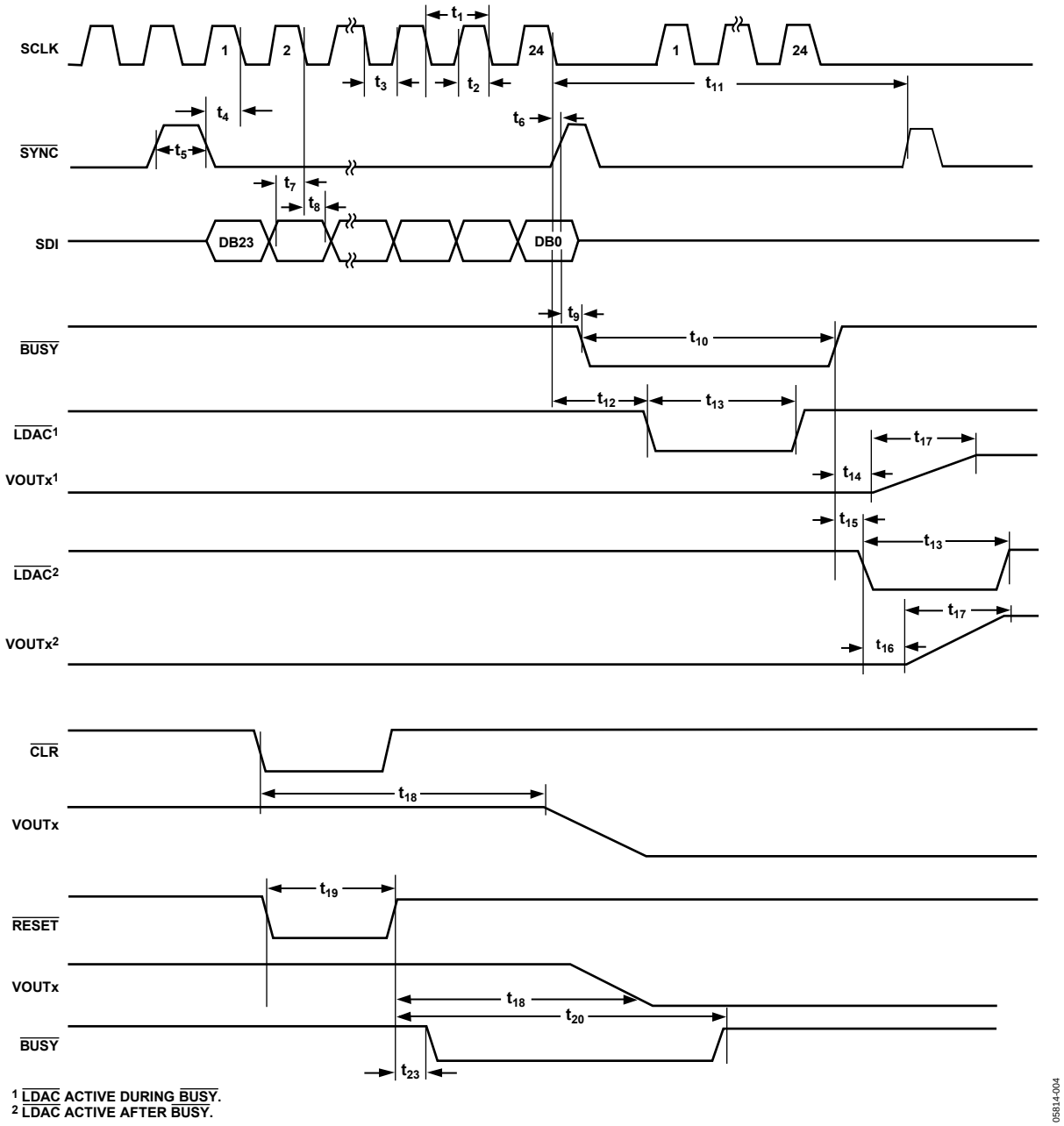


Figure 4. SPI Write Timing

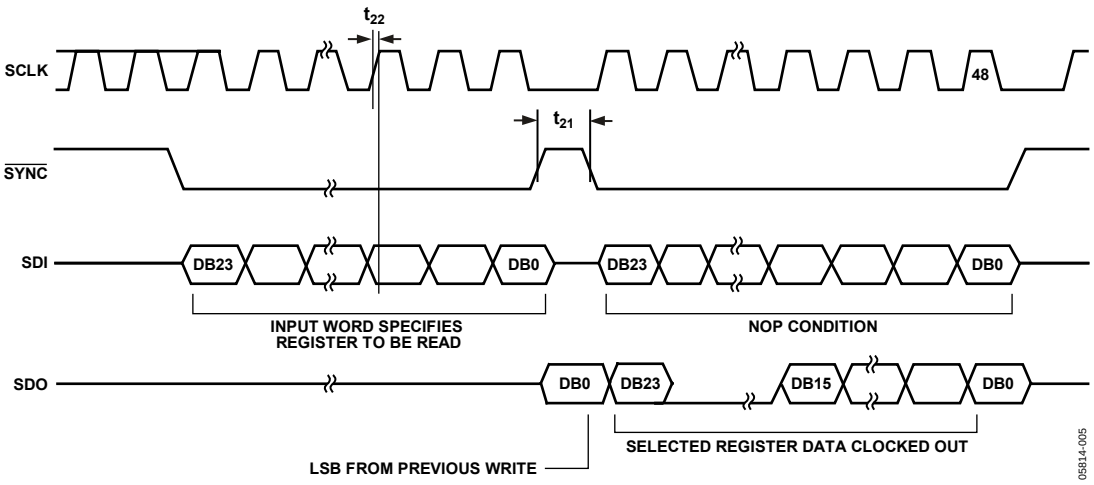


Figure 5. SPI Read Timing

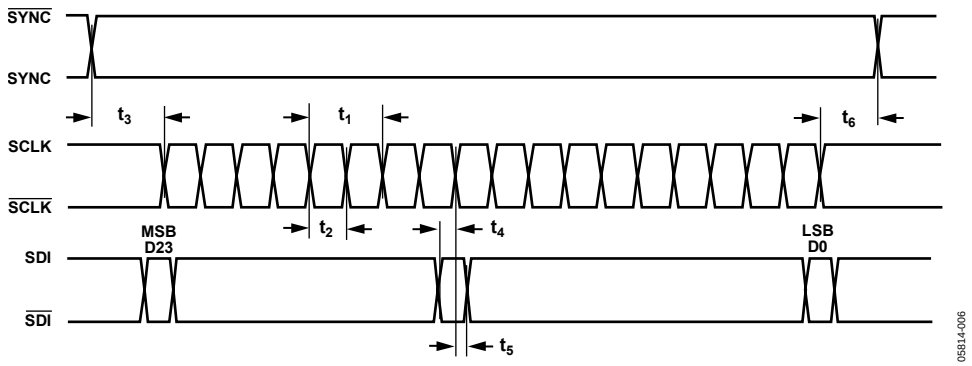


Figure 6. LVDS Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 60 mA do not cause SCR latch-up.

Table 6.

Parameter	Rating
V_{DD} to AGND	−0.3 V to +17 V
V_{SS} to AGND	−17 V to +0.3 V
DV_{CC} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{CC} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV_{CC} + 0.3 V
VREF0, VREF1, VREF2 to AGND	−0.3 V to +5.5 V
VOUT0 through VOUT39 to AGND	V_{SS} − 0.3 V to V_{DD} + 0.3 V
SIGGND0 through SIGGND4 to AGND	−1 V to +1 V
AGND to DGND	−0.3 V to +0.3 V
Operating Temperature Range (T_A)	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature (T_J max)	130°C
θ_{JA} Thermal Impedance	
80-Lead LQFP	38.72°C/W
100-Ball CSP_BGA	40°C/W
Reflow Soldering	
Peak Temperature	230°C
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

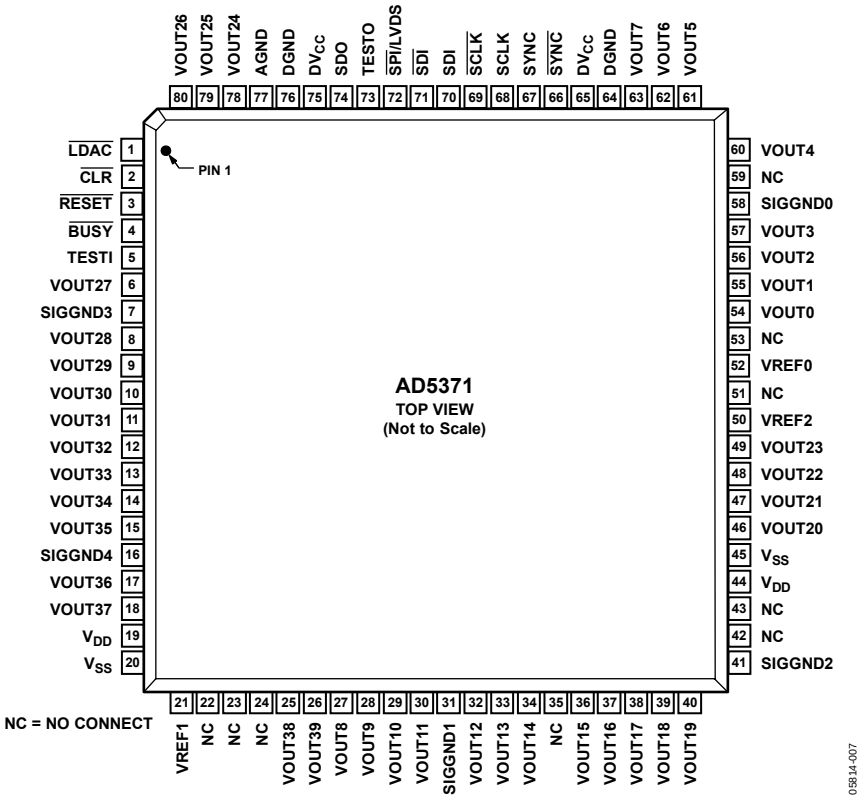


Figure 7. 80-Lead LQFP Pin Configuration

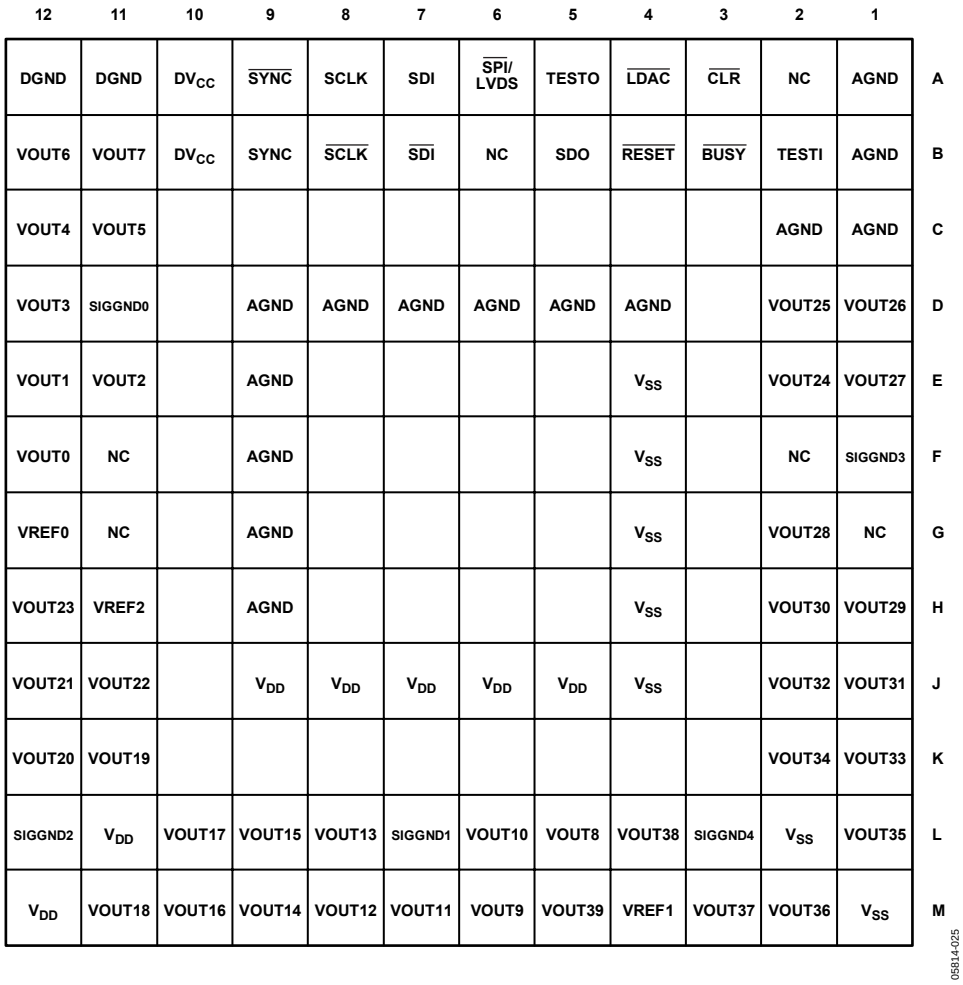


Figure 8. 100-Ball Grid Array Pin Configuration—Bottom View

Table 7. Pin Function Descriptions

Pin No.	Ball No.	Mnemonic	Description
1	A4	$\overline{\text{LDAC}}$	Load DAC Logic Input (Active Low). See the $\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions section for more information.
2	A3	$\overline{\text{CLR}}$	Asynchronous Clear Input (Level Sensitive, Active Low). See the Clear Function section for more information.
3	B4	$\overline{\text{RESET}}$	Digital Reset Input.
4	B3	$\overline{\text{BUSY}}$	Digital Input/Open-Drain Output. $\overline{\text{BUSY}}$ is open drain when an output. See the $\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions section for more information.
5	B2	TESTI	Test Input Pin. Connect this pin to DGND.
73	A5	TESTO	Test Output Pin. This pin remains unconnected.
54 to 57, 60 to 63, 27 to 30, 32 to 34, 36 to 40, 46 to 49, 78 to 80, 6, 8 to 15, 17, 18, 25, 26	F12, E12, E11, D12, C12, C11, B12, B11, L5, M6, L6, M7, M8, L8, M9, L9, M10, L10, M11, K11, K12, J12, J11, H12, E2, D2, D1, E1, G2, H1, H2, J1, J2, K1, K2, L1, M2, M3, L4, M5	VOUT0 to VOUT39	DAC Outputs. Buffered analog outputs for each of the 40 DAC channels. Each analog output is capable of driving an output load of 10 kΩ to ground. Typical output impedance of these amplifiers is 0.5 Ω.

Pin No.	Ball No.	Mnemonic	Description
58	D11	SIGGND0	Reference Ground for DAC 0 to DAC 7. VOUT0 to VOUT7 are referenced to this voltage.
31	L7	SIGGND1	Reference Ground for DAC 8 to DAC 15. VOUT8 to VOUT15 are referenced to this voltage.
41	L12	SIGGND2	Reference Ground for DAC 16 to DAC 23. VOUT16 to VOUT23 are referenced to this voltage.
7	F1	SIGGND3	Reference Ground for DAC 24 to DAC 31. VOUT24 to VOUT31 are referenced to this voltage.
16	L3	SIGGND4	Reference Ground for DAC 32 to DAC 39. VOUT32 to VOUT39 are referenced to this voltage.
52	G12	VREF0	Reference Input for DAC 0 to DAC 7. This reference voltage is referred to AGND.
21	M4	VREF1	Reference Input for DAC 8 to DAC 15. This reference voltage is referred to AGND.
50	H11	VREF2	Reference Input for DAC 16 to DAC 39. This reference voltage is referred to AGND.
19, 44	J5 to J9, L11, M12	V_{DD}	Positive Analog Power Supply; 9 V to 16.5 V for specified performance. Decouple these pins with 0.1 µF ceramic capacitors and 10 µF capacitors.
20, 45	E4, F4, G4, H4, J4, L2, M1	V_{SS}	Negative Analog Power Supply; −16.5 V to −8 V for specified performance. Decouple these pins with 0.1 µF ceramic capacitors and 10 µF capacitors.
64, 76	A11, A12	DGND	Ground for All Digital Circuitry. Connect both DGND pins to the DGND plane.
65, 75	A10, B10	DV_{CC}	Logic Power Supply; 2.5 V to 5.5 V. Decouple these pins with 0.1 µF ceramic capacitors and 10 µF capacitors.
66	A9	$\overline{SYNC}$	Active Low or Differential $\overline{SYNC}$ Input (Complement) for SPI or LVDS Interface. This is the frame synchronization signal for the SPI or LVDS serial interface. See the Timing Characteristics section for more details.
67	B9	SYNC	Differential SYNC Input for LVDS Interface. This is the frame synchronization signal for the LVDS serial interface. See the Timing Characteristics section for more details.
68	A8	SCLK	Serial Clock Input for SPI or LVDS Interface. See the Timing Characteristics section for more details.
69	B8	$\overline{SCLK}$	Differential Serial Clock Input (Complement) for LVDS Interface. See the Timing Characteristics section for more details.
70	A7	SDI	Serial Data Input for SPI or LVDS Interface. See the Timing Characteristics section for more details.
71	B7	$\overline{SDI}$	Differential Serial Data Input (Complement) for LVDS Interface. See the Timing Characteristics section for more details.
72	A6	$\overline{SPI}$/LVDS	Interface Selection Pin. If the pin is low, the SPI interface is selected. If the pin is high, the LVDS interface is selected.
74	B5	SDO	Serial Data Output for SPI Interface. CMOS output. SDO can be used for readback. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
77	A1, B1, C1, C2, D4 to D9, E9, F9, G9, H9	AGND	Ground for All Analog Circuitry. Connect the AGND pin to the AGND plane.
22 to 24, 35, 42, 43, 51, 53, 59	A2, B6, F2, F11, G1, G11	NC	No Connect. Do not connect these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

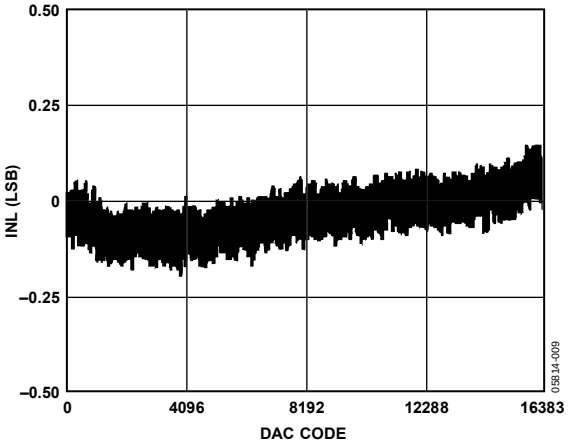


Figure 9. Typical INL Plot

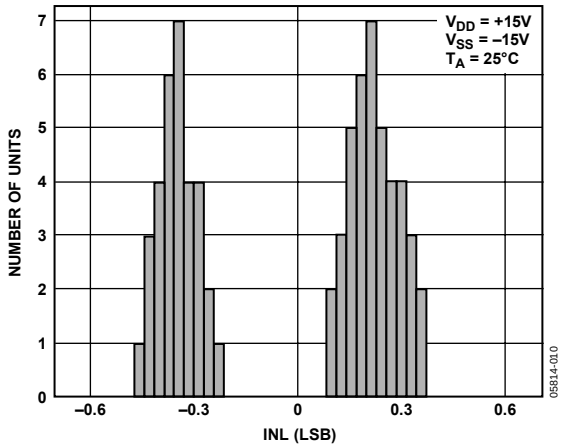


Figure 10. Typical INL Distribution

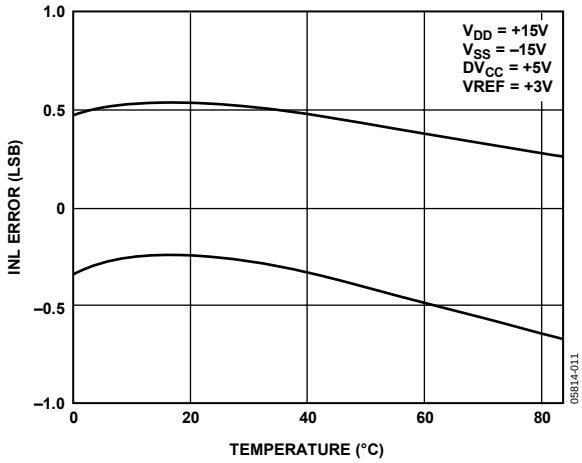


Figure 11. Typical INL Error vs. Temperature

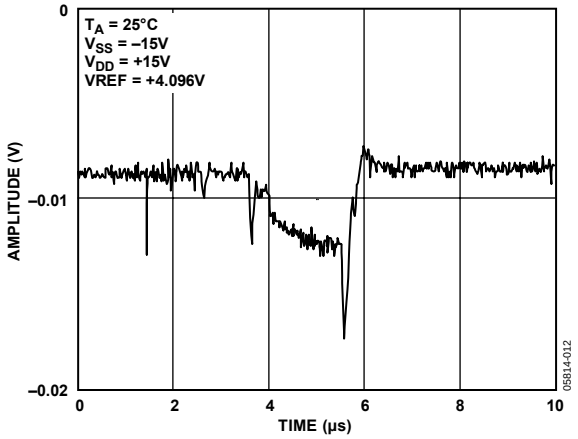


Figure 12. Analog Crosstalk Due to $\overline{LDAC}$

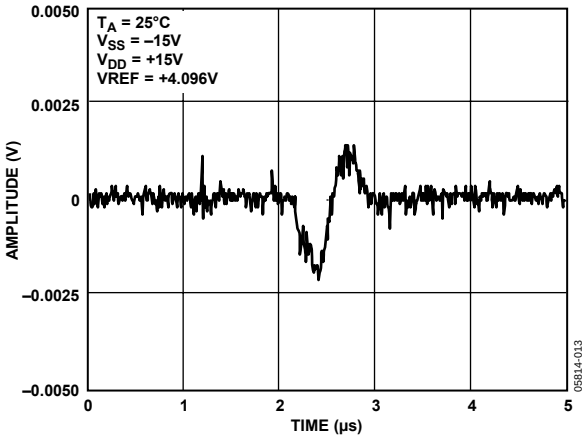


Figure 13. Digital Crosstalk

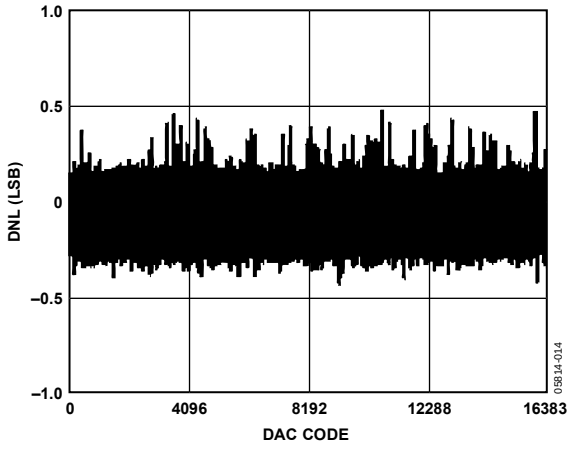


Figure 14. Typical DNL Plot

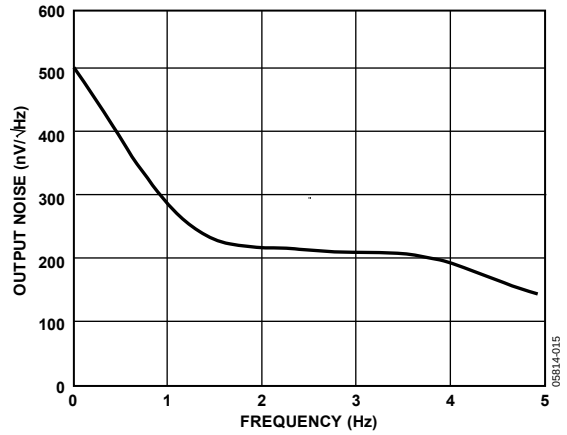


Figure 15. Output Noise Spectral Density

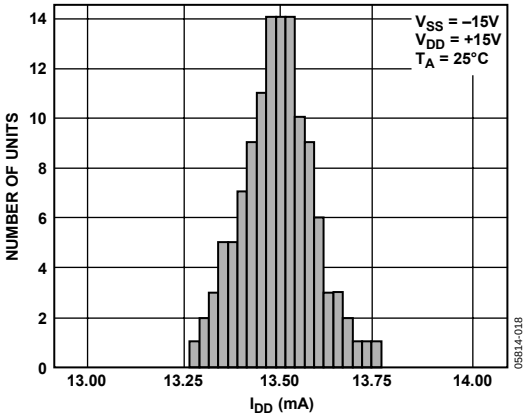


Figure 18. Typical I_{DD} Distribution

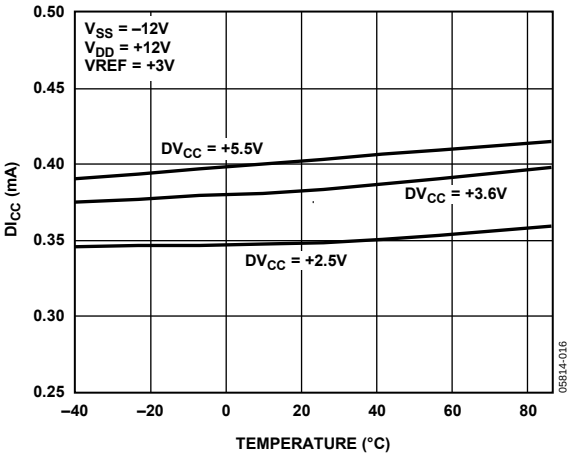


Figure 16. DI_{CC} vs. Temperature

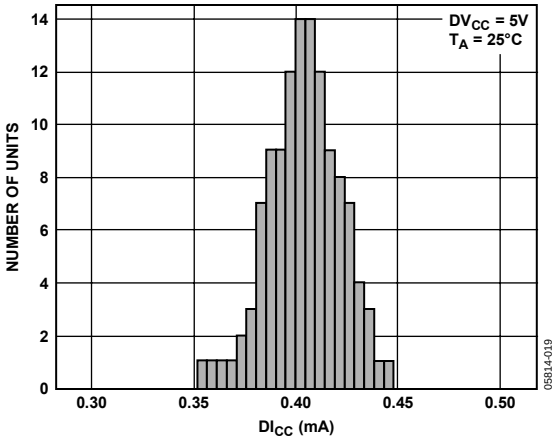


Figure 19. Typical DI_{CC} Distribution

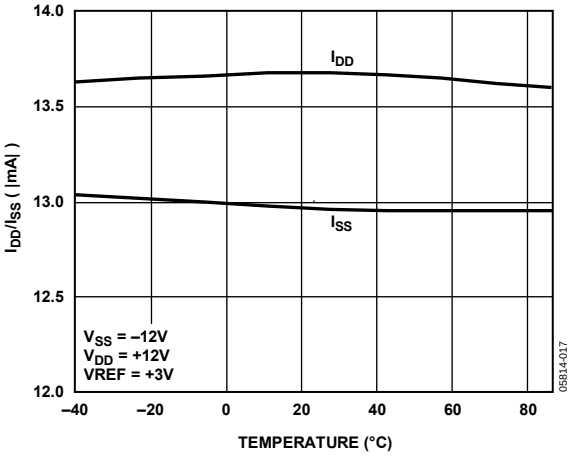


Figure 17. I_{DD}/I_{SS} vs. Temperature

TERMINOLOGY

Integral Nonlinearity (INL)
Integral nonlinearity, or endpoint linearity, is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in least significant bits (LSB).

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error

Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal), expressed in millivolts (mV), when the channel is at its minimum value. Zero-scale error is mainly due to offsets in the output amplifier.

Full-Scale Error
Full-scale error is the error in the DAC output voltage when all 1s are loaded into the DAC register. Full-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal), expressed in millivolts, when the channel is at its maximum value. Full-scale error does not include zero-scale error.

Gain Error
Gain error is the difference between full-scale error and zero-scale error. It is expressed as a percentage of the full-scale range (FSR).

Gain Error = Full-Scale Error − Zero-Scale Error

VOUT Temperature Coefficient
The VOUT temperature coefficient includes output error contributions from linearity, offset, and gain drift.

DC Output Impedance
DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

DC Crosstalk
The DAC outputs are buffered by op amps that share common V_{DD} and V_{SS} power supplies. If the dc load current changes in one channel (due to an update), this change can result in a further dc change in one or more channel outputs. This effect is more significant at high load currents and is reduced as the load currents are reduced. With high impedance loads, the effect is virtually immeasurable. Multiple V_{DD} and V_{SS} terminals are provided to minimize dc crosstalk.

Output Voltage Settling Time
Output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a full-scale input change.

Digital-to-Analog Glitch Energy
Digital-to-analog glitch energy is the amount of energy that is injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

Channel-to-Channel Isolation
Channel-to-channel isolation refers to the proportion of input signal from the reference input of one DAC that appears at the output of another DAC operating from another reference. It is expressed in decibels and measured at midscale.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one converter due to both the digital change and subsequent analog output change at another converter. It is specified in nV-s.

Digital Crosstalk
Digital crosstalk is defined as the glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter. It is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the digital inputs of the device can be capacitively coupled both across and through the device to appear as noise on the VOUTx pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
Output noise spectral density is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz.

THEORY OF OPERATION

DAC ARCHITECTURE

The AD5371 contains 40 DAC channels and 40 output amplifiers in a single package. The architecture of a single DAC channel consists of a 14-bit resistor-string DAC followed by an output buffer amplifier. The resistor-string section is simply a string of resistors, of equal value, from VREFx to AGND. This type of architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The output amplifier multiplies the DAC output voltage by 4. The nominal output span is 12 V with a 3 V reference and 20 V with a 5 V reference.

CHANNEL GROUPS

The 40 DAC channels of the AD5371 are arranged into five groups of eight channels. The eight DACs of Group 0 derive their reference voltage from VREF0. The eight DACs of Group 1 derive their reference voltage from VREF1. Group 2 to Group 4 derive their reference voltage from VREF2. Each group has its own signal ground pin.

Table 8. Register Descriptions

Register Name	Word Length (Bits)	Default Value	Description
X1A	14	0x1555	Input Data Register A. One for each DAC channel.
X1B	14	0x1555	Input Data Register B. One for each DAC channel.
M	14	0x3FFF	Gain trim registers. One for each DAC channel.
C	14	0x2000	Offset trim registers. One for each DAC channel.
X2A	14	Not user accessible	Output Data Register A. One for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable or directly writable.
X2B	14	Not user accessible	Output Data Register B. One for each DAC channel. These registers store the final, calibrated DAC data after gain and offset trimming. They are not readable or directly writable.
DAC		Not user accessible	Data registers from which the DACs take their final input data. The DAC registers are updated from the X2A or X2B register. They are not readable or directly writable.
OFS0	14	0x1555	Offset DAC 0 data register. Sets offset for Group 0.
OFS1	14	0x1555	Offset DAC 1 data register. Sets offset for Group 1.
OFS2	14	0x1555	Offset DAC 2 data register. Sets offset for Group 2 to Group 4.
Control	3	0x00	Bit 2 = $\overline{A}$/B. 0 = global selection of X1A input data registers. 1 = global selection of X1B input data registers. Bit 1 = enable thermal shutdown. 0 = disable thermal shutdown. 1 = enable thermal shutdown. Bit 0 = software power-down. 0 = software power-up. 1 = software power-down.
A/B Select 0	8	0x00	Each bit in this register determines if a DAC in Group 0 takes its data from Register X2A or Register X2B. 0 = X2A. 1 = X2B.
A/B Select 1	8	0x00	Each bit in this register determines if a DAC in Group 1 takes its data from Register X2A or Register X2B. 0 = X2A. 1 = X2B.
A/B Select 2	8	0x00	Each bit in this register determines if a DAC in Group 2 takes its data from Register X2A or Register X2B. 0 = X2A. 1 = X2B.
A/B Select 3	8	0x00	Each bit in this register determines if a DAC in Group 3 takes its data from Register X2A or Register X2B. 0 = X2A. 1 = X2B.
A/B Select 4	8	0x00	Each bit in this register determines if a DAC in Group 4 takes its data from Register X2A or Register X2B. 0 = X2A. 1 = X2B.

A/B REGISTERS AND GAIN/OFFSET ADJUSTMENT

Each DAC channel has seven data registers. The actual DAC data-word can be written to either the X1A or the X1B input register, depending on the setting of the $\overline{A}$/B bit in the control register. If the $\overline{A}$/B bit is 0, data is written to the X1A register. If the $\overline{A}$/B bit is 1, data is written to the X1B register. Note that this single bit is a global control and affects every DAC channel in the device. It is not possible to set up the device on a per-channel basis so that some writes are to X1A registers and some writes are to X1B registers.

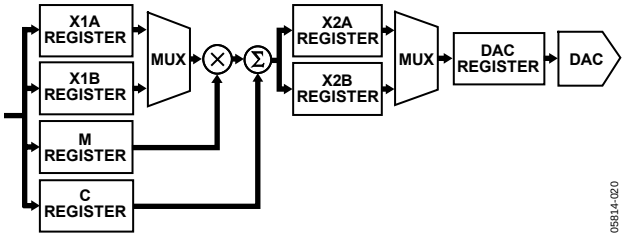


Figure 20. Data Registers Associated with Each DAC Channel

Each DAC channel also has a gain (M) register and an offset (C) register that allow trimming out of the gain and offset errors of the entire signal chain. Data from the X1A register is operated on by a digital multiplier and adder controlled by the contents of the M and C registers. The calibrated DAC data is then stored in the X2A register. Similarly, data from the X1B register is operated on by the multiplier and adder and stored in the X2B register.

Although Figure 20 shows a multiplier and adder for each channel, there is only one multiplier and one adder in the device shared among all channels. This has implications for the update speed when several channels are updated simultaneously, as described in the Register Update Rates section.

Each time data is written to the X1A register, or to the M or C register with the $\overline{A}$/B control bit set to 0, the X2A data is recalculated and the X2A register is automatically updated. Similarly, X2B is updated each time data is written to X1B, or to M or C with $\overline{A}$/B set to 1. The X2A and X2B registers are not readable or directly writable by the user.

Data output from the X2A and X2B registers is routed to the final DAC register by a multiplexer. Whether each individual DAC takes its data from the X2A or X2B register is controlled by an 8-bit A/B select register associated with each group of eight DACs. If a bit in this register is 0, the DAC takes its data from the X2A register; if 1, the DAC takes its data from the X2B register (Bit 0 through Bit 7 control DAC 0 to DAC 7).

Note that because there are 40 bits in five registers, it is possible to set up, on a per-channel basis, whether each DAC takes its data from the X2A or X2B register. A global command is also provided that sets all bits in the A/B select registers to 0 or to 1.

LOAD DAC

All DACs in the AD5371 can be updated simultaneously by taking $\overline{LDAC}$ low when each DAC register is updated from either its X2A or X2B register, depending on the setting of the A/B select registers. The DAC register is not readable or directly writable by the user. $\overline{LDAC}$ can be permanently tied low, and the DAC output is updated whenever new data appears in the appropriate DAC register.

OFFSET DACS

In addition to the gain and offset trim for each DAC, there are three 14-bit offset DACs, one for Group 0, one for Group 1, and one for Group 2 to Group 4. These allow the output range of all DACs connected to them to be offset within a defined range. Thus, subject to the limitations of headroom, it is possible to set the output range of Group 0, Group 1, or Group 2 to Group 4 to be unipolar positive, unipolar negative, or bipolar, either symmetrical or asymmetrical about 0 V. The DACs in the AD5371 are factory trimmed with the offset DACs set at their default values. This results in optimum offset and gain performance for the default output range and span.

When the output range is adjusted by changing the value of the offset DAC, an extra offset is introduced due to the gain error of the offset DAC. The amount of offset is dependent on the magnitude of the reference and how much the offset DAC deviates from its default value. See the Specifications section for this offset. The worst-case offset occurs when the offset DAC is at positive or negative full scale. This value can be added to the offset present in the main DAC channel to give an indication of the overall offset for that channel. In most cases, the offset can be removed by programming the C register of the channel with an appropriate value. The extra offset caused by the offset DAC needs to be taken into account only when the offset DAC is changed from its default value. Figure 21 shows the allowable code range that can be loaded to the offset DAC, depending on the reference value used. Thus, for a 5 V reference, the offset DAC should not be programmed with a value greater than 8192 (0x2000).

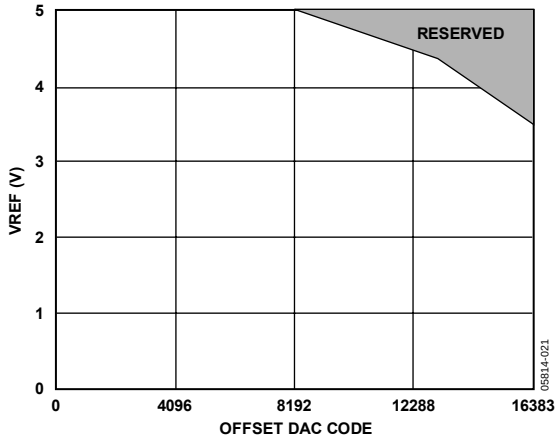


Figure 21. Offset DAC Code Range

OUTPUT AMPLIFIER

The output amplifiers can swing to 1.4 V below the positive supply and 1.4 V above the negative supply, which limits how much the output can be offset for a given reference voltage. For example, it is not possible to have a unipolar output range of 20 V, because the maximum supply voltage is ±16.5 V.

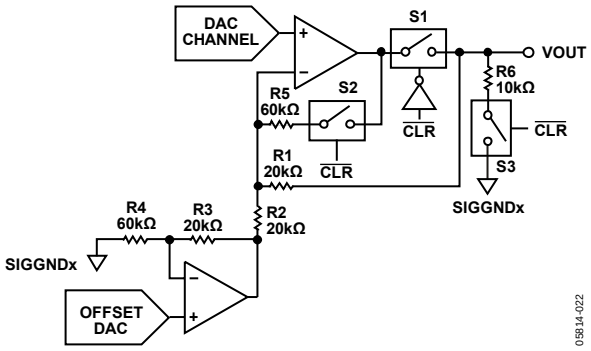


Figure 22. Output Amplifier and Offset DAC

Figure 22 shows details of a DAC output amplifier and its connections to its corresponding offset DAC. On power-up, S1 is open, disconnecting the amplifier from the output. S3 is closed, so the output is pulled to the corresponding SIGGNDx (R1 and R2 are greater than R6). S2 is also closed to prevent the output amplifier from being open-loop. If $\overline{\text{CLR}}$ is low at power-up, the output remains in this condition until $\overline{\text{CLR}}$ is taken high. The DAC registers can be programmed, and the outputs assume the programmed values when $\overline{\text{CLR}}$ is taken high. Even if $\overline{\text{CLR}}$ is high at power-up, the output remains in this condition until $V_{DD} > 6$ V and $V_{SS} < -4$ V and the initialization sequence has finished. The outputs then go to their power-on default value.

TRANSFER FUNCTION

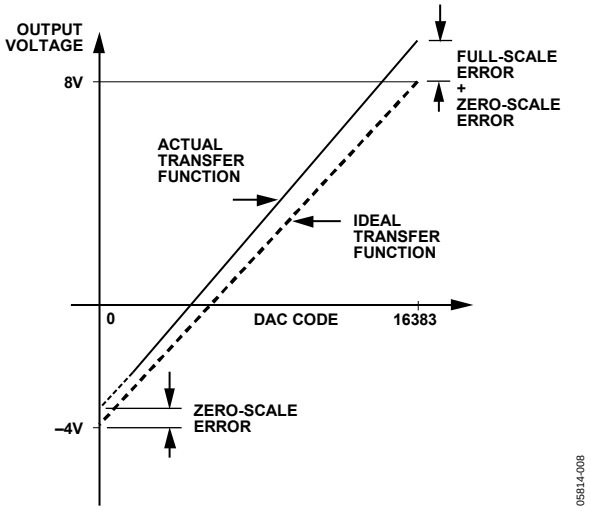


Figure 23. DAC Transfer Function

The output voltage of a DAC in the AD5371 is dependent on the value in the input register, the value of the M and C registers, and the value in the offset DAC.

The input code is the value in the X1A or X1B register that is applied to the DAC (X1A, X1B default code = 5461).

$$DAC\_CODE = INPUT\_CODE \times (M + 1)/2^{14} + C - 2^{13}.$$

where:
M = code in gain register − default code = $2^{14} - 1$.
C = code in offset register − default code = 2^{13}.

The DAC output voltage is calculated as follows:

$$VOUT = 4 \times VREFx \times (DAC\_CODE - OFFSET\_CODE)/2^{14} + V_{SIGGND}$$

where:
DAC_CODE should be within the range of 0 to 16,383.
VREF = 3.0 V for a 12 V span and 5.0 V for a 20 V span.
OFFSET_CODE is the code loaded to the offset DAC. On power-up, the default code loaded to the offset DAC is 5461 (0x1555). With a 3 V reference, this gives a span of −4 V to +8 V.

REFERENCE SELECTION

The AD5371 has three reference input pins. The voltage applied to the reference pins determines the output voltage span on VOUT0 to VOUT39. VREF0 determines the voltage span for VOUT0 to VOUT7 (Group 0), VREF1 determines the voltage span for VOUT8 to VOUT15 (Group 1), and VREF2 determines the voltage span for VOUT16 to VOUT39 (Group 2 to Group 4). The reference voltage applied to each VREF pin can be different, if required, allowing each group to have a different voltage span. The output voltage range and span can be adjusted further by programming the offset and gain registers for each channel and by programming the offset DACs. If the offset and gain features are not used (that is, the M and C registers are left at their default values), the required reference levels can be calculated as follows:

$$VREF = (VOUT_{MAX} - VOUT_{MIN})/4$$

If the offset and gain features of the AD5371 are used, the required output range is slightly different. The selected output range should take into account the system offset and gain errors that need to be trimmed out. Therefore, the selected output range should be larger than the actual required range.

Calculate the required reference levels as follows:

1. Identify the nominal output range on VOUT.
2. Identify the maximum offset span and the maximum gain required on the full output signal range.
3. Calculate the new maximum output range on VOUT, including the expected maximum offset and gain errors.
4. Choose the new required $VOUT_{MAX}$ and $VOUT_{MIN}$, keeping the VOUT limits centered on the nominal values. Note that V_{DD} and V_{SS} must provide sufficient headroom.
5. Calculate the value of VREF as follows:

$$VREF = (VOUT_{MAX} - VOUT_{MIN})/4$$

Reference Selection Example

If

Nominal output range = 12 V (−4 V to +8 V)

Zero-scale error = ±70 mV

Gain error = ±3%, and

SIGGNDx = AGND = 0 V

Then

Gain error = ±3%
=> Maximum positive gain error = 3%
=> Output range including gain error = 12 + 0.03(12) = 12.36 V

Zero-scale error = ±70 mV
=> Maximum offset error span = 2(70 mV) = 0.14 V
=> Output range including gain error and zero-scale error = 12.36 V + 0.14 V = 12.5 V

VREF calculation

Actual output range = 12.5 V, that is, −4.25 V to +8.25 V;
VREF = (8.25 V + 4.25 V)/4 = 3.125 V

If the solution yields an inconvenient reference level, the user can adopt one of the following approaches:

- Use a resistor divider to divide down a convenient, higher reference level to the required level.
- Select a convenient reference level above VREF and modify the gain and offset registers to digitally downsize the reference. In this way, the user can use almost any convenient reference level but can reduce the performance by overcompaction of the transfer function.
- Use a combination of these two approaches.

CALIBRATION

The user can perform a system calibration on the AD5371 to reduce gain and offset errors to below 1 LSB. This reduction is achieved by calculating new values for the M and C registers and reprogramming them.

The M and C registers should not be programmed until both the zero-scale and full-scale errors are calculated.

Reducing Zero-Scale Error

Zero-scale error can be reduced as follows:

1. Set the output to the lowest possible value.
2. Measure the actual output voltage and compare it to the required value. This gives the zero-scale error.
3. Calculate the number of LSBs equivalent to the error and add this number to the default value of the C register. Note that only negative zero-scale error can be reduced.

Reducing Full-Scale Error

Full-scale error can be reduced as follows:

1. Measure the zero-scale error.
2. Set the output to the highest possible value.
3. Measure the actual output voltage and compare it to the required value. Add this error to the zero-scale error. This is the span error, which includes the full-scale error.
4. Calculate the number of LSBs equivalent to the span error and subtract this number from the default value of the M register. Note that only positive full-scale error can be reduced.

AD5371 Calibration Example

This example assumes that a −4 V to +8 V output is required. The DAC output is set to −4 V but measured at −4.03 V. This gives a zero-scale error of −30 mV.

1 LSB = 12 V/16,384 = 732.42 μV

30 mV = 41 LSBs

The full-scale error can now be calculated. The output is set to 8 V and a value of 8.02 V is measured. This gives a full-scale error of +20 mV and a span error of +20 mV − (−30 mV) = +50 mV.

50 mV = 68 LSBs

The errors can now be removed as follows:

1. Add 41 LSBs to the default C register value:
   8192 + 41 = 8233
2. Subtract 68 LSBs from the default M register value:
   16,383 − 68 = 16,315
3. Program the M register to 16,315; program the C register to 8233.

ADDITIONAL CALIBRATION

The techniques described in the previous section are usually enough to reduce the zero-scale and full-scale errors in most applications. However, there are limitations whereby the errors may not be sufficiently reduced. For example, the offset (C) register can only be used to reduce the offset caused by the negative zero-scale error. A positive offset cannot be reduced. Likewise, if the maximum voltage is below the ideal value, that is, a negative full-scale error, the gain (M) register cannot be used to increase the gain to compensate for the error.

These limitations can be overcome by increasing the reference value. With a 3 V reference, a 12 V span is achieved. The ideal voltage range for the AD5371 is −4 V to +8 V. Using a +3.1 V reference increases the range to −4.133 V to +8.2667 V. Clearly, in this case, the offset and gain errors are insignificant, and the M and C registers can be used to raise the negative voltage to −4 V and then reduce the maximum voltage to +8 V to give the most accurate values possible.

RESET FUNCTION

The reset function is initiated by the $\overline{\text{RESET}}$ pin. On the rising edge of $\overline{\text{RESET}}$, the AD5371 state machine initiates a reset sequence to reset the X, M, and C registers to their default values. This sequence typically takes 300 µs, and the user should not write to the part during this time. On power-up, it is recommended that the user bring $\overline{\text{RESET}}$ high as soon as possible to properly initialize the registers.

When the reset sequence is complete (and provided that $\overline{\text{CLR}}$ is high), the DAC output is at a potential specified by the default register settings, which is equivalent to SIGGNDx. The DAC outputs remain at SIGGNDx until the X, M, or C register is updated and $\overline{\text{LDAC}}$ is taken low. The AD5371 can be returned to the default state by pulsing $\overline{\text{RESET}}$ low for at least 30 ns. Note that, because the reset function is triggered by the rising edge, bringing $\overline{\text{RESET}}$ low has no effect on the operation of the AD5371.

CLEAR FUNCTION

$\overline{\text{CLR}}$ is an active low input that should be high for normal operation. The $\overline{\text{CLR}}$ pin has an internal 500 kΩ pull-down resistor. When $\overline{\text{CLR}}$ is low, the input to each of the DAC output buffer stages, VOUT0 to VOUT39, is switched to the externally set potential on the relevant SIGGNDx pin. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is taken high again, the DAC outputs return to their previous values. The contents of the input registers and the DAC registers are not affected by taking $\overline{\text{CLR}}$ low. To prevent glitches from appearing on the outputs, bring $\overline{\text{CLR}}$ low before writing to the offset DAC to adjust the output span.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

The value of an X2 (A or B) register is calculated each time the user writes new data to the corresponding X1, C, or M register. During the calculation of X2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the X1, M, or C register (see the Register Update Rates section for more details), but no DAC output updates can take place.

The $\overline{\text{BUSY}}$ pin is bidirectional and has a 50 kΩ internal pull-up resistor. When multiple AD5371 devices are used in one system, the $\overline{\text{BUSY}}$ pins can be tied together. This is useful when it is required that no DAC in any device be updated until all other DACs are ready to be updated. When each device has finished updating the X2 (A or B) register, it releases the $\overline{\text{BUSY}}$ pin. If another device has not finished updating its X2 register, it holds $\overline{\text{BUSY}}$ low, thus delaying the effect of $\overline{\text{LDAC}}$ going low.

The DAC outputs are updated by taking the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored and the DAC outputs are updated immediately after $\overline{\text{BUSY}}$ goes high. A user can also hold the $\overline{\text{LDAC}}$ input permanently low. In this case, the DAC outputs are updated immediately after $\overline{\text{BUSY}}$ goes high. Whenever the A/B select registers are written to, $\overline{\text{BUSY}}$ also goes low for approximately 500 ns.

The AD5371 has flexible addressing that allows writing of data to a single channel, all channels in a group, the same channel in Group 0 to Group 4, the same channel in Group 1 to Group 4, or all channels in the device. This means that 1, 4, 5, 8, or 40 DAC register values may need to be calculated and updated. Because there is only one multiplier shared among 40 channels, this task must be done sequentially so that the length of the $\overline{\text{BUSY}}$ pulse varies according to the number of channels being updated.

Table 9. $\overline{\text{BUSY}}$ Pulse Widths

Action	$\overline{\text{BUSY}}$ Pulse Width[1]
Loading X1A, X1B, C, or M to 1 channel[2]	1.5 µs maximum
Loading X1A, X1B, C, or M to 5 channels	3.9 µs maximum
Loading X1A, X1B, C, or M to 8 channels	5.7 µs maximum
Loading X1A, X1B, C, or M to 40 channels	24.9 µs maximum

[1] $\overline{\text{BUSY}}$ pulse width = ((number of channels + 1) × 600 ns) + 300 ns.
[2] A single channel update is typically 1 µs.

The AD5371 contains an extra feature whereby a DAC register is not updated unless its X2A or X2B register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the X2A or X2B register, depending on the setting of the A/B select registers. However, the AD5371 updates the DAC register only if the X2A or X2B data has changed, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODE

The AD5371 can be powered down by setting Bit 0 in the control register to 1. This turns off the DACs, thus reducing the current consumption. The DAC outputs are connected to their respective SIGGNDx potentials. The power-down mode does not change the contents of the registers, and the DACs return to their previous voltage when the power-down bit is cleared to 0.

THERMAL SHUTDOWN FUNCTION

The AD5371 can be programmed to shut down the DACs if the temperature on the die exceeds 130°C. Setting Bit 1 in the control register to 1 enables this function (see Table 17). If the die temperature exceeds 130°C, the AD5371 enters a thermal shutdown mode that is equivalent to setting the power-down bit in the control register to 1. To indicate that the AD5371 has entered thermal shutdown mode, Bit 4 of the control register is set to 1. The AD5371 remains in thermal shutdown mode, even if the die temperature falls, until Bit 1 in the control register is cleared to 0.

TOGGLE MODE

The AD5371 has two X2 registers per channel, X2A and X2B, that can be used to switch the DAC output between two levels with ease. This approach greatly reduces the overhead required by a microprocessor, which would otherwise need to write to each channel individually. When the user writes to the X1A, X1B, M, or C register, the calculation engine takes a certain amount of time to calculate the appropriate X2A or X2B value. If an application, such as a data generator, requires that the DAC output switch between two levels only, any method that reduces the amount of calculation time necessary is advantageous.

For the data generator example, the user needs only to set the high and low levels for each channel once by writing to the X1A and X1B registers. The values of X2A and X2B are calculated and stored in their respective registers. The calculation delay, therefore, happens only during the setup phase, that is, when programming the initial values. To toggle a DAC output between the two levels, it is only required to write to the relevant A/B select register to set the MUX2 register bit. Furthermore, because there are eight MUX2 control bits per register, it is possible to update eight channels with a single write. Table 10 shows the bits that correspond to each DAC output.

Table 10. DACs Selected by A/B Select Registers

A/B Select Register	Bits[1]							
	F7	F6	F5	F4	F3	F2	F1	F0
0	VOUT7	VOUT6	VOUT5	VOUT4	VOUT3	VOUT2	VOUT1	VOUT0
1	VOUT15	VOUT14	VOUT13	VOUT12	VOUT11	VOUT10	VOUT9	VOUT8
2	VOUT23	VOUT22	VOUT21	VOUT20	VOUT19	VOUT18	VOUT17	VOUT16
3	VOUT31	VOUT30	VOUT29	VOUT28	VOUT27	VOUT26	VOUT25	VOUT24
4	VOUT39	VOUT38	VOUT37	VOUT36	VOUT35	VOUT34	VOUT33	VOUT32

[1] If the bit is set to 0, Register X2A is selected. If the bit is set to 1, Register X2B is selected.

SERIAL INTERFACE

The AD5371 contains two high speed serial interfaces: an SPI-compatible interface operating at clock frequencies up to 50 MHz (20 MHz for read operations) and an LVDS interface. To minimize both the power consumption of the device and the on-chip digital noise, the interface powers up fully only when the device is being written to, that is, on the falling edge of $\overline{\text{SYNC}}$.

SPI INTERFACE

The serial interface is 2.5 V LVTTL-compatible when operating from a 2.5 V to 3.6 V DV_{CC} supply. The SPI interface is selected when the $\overline{\text{SPI}}$/LVDS pin is held low. It is controlled by four pins, as described in Table 11.

Table 11. Pins That Control the SPI Interface

Pin	Description
$\overline{\text{SYNC}}$	Frame synchronization input
SDI	Serial data input pin
SCLK	Clocks data in and out of the device
SDO	Serial data output pin for data readback

When the SPI mode is used, the SYNC, $\overline{\text{SDI}}$, and $\overline{\text{SCLK}}$ pins should be connected to DGND either directly or by using pull-down resistors.

LVDS INTERFACE

The LVDS interface uses the same input pins, with the same designations, as the SPI interface; however, SDO is not used. In addition, three other pins are provided for the complementary signals needed for differential operation, as described in Table 12.

Table 12. Pins That Control the LVDS Interface

Pin	Description
SYNC	Differential frame synchronization signal
$\overline{\text{SYNC}}$	Differential frame synchronization signal (complement)
SDI	Differential serial data input
$\overline{\text{SDI}}$	Differential serial data input (complement)
SCLK	Differential serial clock input
$\overline{\text{SCLK}}$	Differential serial clock input (complement)

SPI WRITE MODE

The AD5371 allows writing of data via the serial interface to every register directly accessible to the serial interface, that is, all registers except the X2A, X2B, and DAC registers. The X2A and X2B registers are updated when the user writes to the X1A, X1B, M, or C register, and the DAC data registers are updated by $\overline{\text{LDAC}}$.

The serial word (see Table 13) is 24 bits long: 14 of these bits are data bits; six bits are address bits; two bits are mode bits that determine what is done with the data; and two bits are reserved.

The serial interface works with both a continuous and a burst (gated) serial clock. Serial data applied to SDI is clocked into the AD5371 by clock pulses applied to SCLK. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. At least 24 falling clock edges must be applied to SCLK to clock in 24 bits of data before $\overline{\text{SYNC}}$ is taken high again. If $\overline{\text{SYNC}}$ is taken high before the 24th falling clock edge, the write operation is aborted.

If a continuous clock is used, $\overline{\text{SYNC}}$ must be taken high before the 25th falling clock edge. This inhibits the clock within the AD5371. If more than 24 falling clock edges are applied before $\overline{\text{SYNC}}$ is taken high again, the input data becomes corrupted. If an externally gated clock of exactly 24 pulses is used, $\overline{\text{SYNC}}$ can be taken high any time after the 24th falling clock edge.

The input register addressed is updated on the rising edge of $\overline{\text{SYNC}}$. For another serial transfer to take place, $\overline{\text{SYNC}}$ must be taken low again.

Table 13. Serial Word Bit Assignment

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1[1]	I0[1]
M1	M0	A5	A4	A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	0	0

[1] Bit I1 and Bit I0 are reserved for future use and should be set to 0 when writing the serial word. These bits read back as 0.

SPI READBACK MODE

The AD5371 allows data readback via the serial interface from every register directly accessible to the serial interface, that is, all registers except the X2A, X2B, and DAC data registers. To read back a register, it is first necessary to tell the AD5371 which register is to be read. This is achieved by writing a word whose first two bits are the Special Function Code 00 to the device. The remaining bits then determine which register is to be read back.

If a readback command is written to a special function register, data from the selected register is clocked out of the SDO pin during the next SPI operation. The SDO pin is normally three-stated but becomes driven as soon as a read command is issued. The pin remains driven until the register data is clocked out. See Figure 5 for the read timing diagram. Note that due to the timing requirements of t_{22} (25 ns), the maximum speed of the SPI interface during a read operation should not exceed 20 MHz.

LVDS OPERATION

The LVDS interface operates as follows. Note that, because the LVDS signals are differential, when a signal goes high, its complementary signal goes low, and vice versa.

1. The $\overline{\text{SYNC}}$ signal frames the data. SCLK is initially high.
2. After $\overline{\text{SYNC}}$ goes high and the $\overline{\text{SYNC}}$-to-SCLK setup time has elapsed, SCLK can start to clock in the data.
3. Data is clocked into the AD5371 on the high-to-low transition of SCLK and must be stable at this time (observe setup and hold time specifications).
4. $\overline{\text{SYNC}}$ can then be taken low after the SCLK-to-$\overline{\text{SYNC}}$ hold time to latch the data.

The same comments about burst and continuous clocks for the SPI interface apply to the LVDS interface. However, readback is not available when using the LVDS interface.

REGISTER UPDATE RATES

The value of the X2A register or the X2B register is calculated each time the user writes new data to the corresponding X1, C, or M register. The calculation is performed by a three-stage process. The first two stages take approximately 600 ns each, and the third stage takes approximately 300 ns. When the write to the X1, C, or M register is complete, the calculation process begins. If the write operation involves the update of a single DAC channel, the user is free to write to another register, provided that the write operation does not finish until the first-stage calculation is complete, that is, 600 ns after the completion of the first write operation. If a group of channels is being updated by a single write operation, the first-stage calculation is repeated for each channel, taking 600 ns per channel. In this case, the user should not complete the next write operation until this time has elapsed.

CHANNEL ADDRESSING AND SPECIAL MODES

If the mode bits are not 00, the data-word D13 to D0 is written to the device. Address Bit A5 to Address Bit A0 determine which channels are written to, and the mode bits determine to which register (X1A, X1B, C, or M) the data is written, as shown in Table 14 and Table 15. Data is to be written to the X1A register when the $\overline{\text{A}}$/B bit in the control register is 0, or to the X1B register when the $\overline{\text{A}}$/B bit is 1.

Table 14. Mode Bits

M1	M0	Action
1	1	Write to DAC input data (X) register
1	0	Write to DAC offset (C) register
0	1	Write to DAC gain (M) register
0	0	Special function, used in combination with other bits of the data-word

The AD5371 has very flexible addressing that allows the writing of data to a single channel, all channels in a group, the same channel in Group 0 to Group 4, the same channel in Group 1 to Group 4, or all channels in the device (see Table 15).

Table 15 shows which groups and which channels are addressed for every combination of Address Bit A5 to Address Bit A0.

Table 15. Group and Channel Addressing

Address Bit A2 to Address Bit A0	Address Bit A5 to Address Bit A3							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
000	All groups, all channels	Group 0, Channel 0	Group 1, Channel 0	Group 2, Channel 0	Group 3, Channel 0	Group 4, Channel 0	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 0	Group 1, Group 2, Group 3, Group 4; Channel 0
000	Group 0, all channels	Group 0, Channel 1	Group 1, Channel 1	Group 2, Channel 1	Group 3, Channel 1	Group 4, Channel 1	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 1	Group 1, Group 2, Group 3, Group 4; Channel 1
010	Group 1, all channels	Group 0, Channel 2	Group 1, Channel 2	Group 2, Channel 2	Group 3, Channel 2	Group 4, Channel 2	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 2	Group 1, Group 2, Group 3, Group 4; Channel 2
011	Group 2, all channels	Group 0, Channel 3	Group 1, Channel 3	Group 2, Channel 3	Group 3, Channel 3	Group 4, Channel 3	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 3	Group 1, Group 2, Group 3, Group 4; Channel 3
100	Group 3, all channels	Group 0, Channel 4	Group 1, Channel 4	Group 2, Channel 4	Group 3, Channel 4	Group 4, Channel 4	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 4	Group 1, Group 2, Group 3, Group 4; Channel 4
101	Group 4, all channels	Group 0, Channel 5	Group 1, Channel 5	Group 2, Channel 5	Group 3, Channel 5	Group 4, Channel 5	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 5	Group 1, Group 2, Group 3, Group 4; Channel 5
110	Reserved	Group 0, Channel 6	Group 1, Channel 6	Group 2, Channel 6	Group 3, Channel 6	Group 4, Channel 6	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 6	Group 1, Group 2, Group 3, Group 4; Channel 6
111	Reserved	Group 0, Channel 7	Group 1, Channel 7	Group 2, Channel 7	Group 3, Channel 7	Group 4, Channel 7	Group 0, Group 1, Group 2, Group 3, Group 4; Channel 7	Group 1, Group 2, Group 3, Group 4; Channel 7

SPECIAL FUNCTION MODE

If the mode bits are 00, the special function mode is selected, as shown in Table 16. Bit I21 to Bit I16 of the serial data-word select the special function, and the remaining bits are data required for execution of the special function, for example, the channel address for data readback. The codes for the special functions are shown in Table 17. Table 18 shows the addresses for data readback.

Table 16. Special Function Mode

I23	I22	I21	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
0	0	S5	S4	S3	S2	S1	S0	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

Table 17. Special Function Codes

Special Function Code							
S5	S4	S3	S2	S1	S0	Data (F15 to F0)	Action
0	0	0	0	0	0	0000 0000 0000 0000	No operation (NOP).
0	0	0	0	0	1	XXXX XXXX XXXX X[F2:F0]	Write control register. F4 = overtemperature indicator (read-only bit). This bit should be 0 when writing to the control register. F3 = reserved. This bit should be 0 when writing to the control register. F2 = 1: Select Register X1B for input. F2 = 0: Select Register X1A for input. F1 = 1: Enable thermal shutdown mode. F1 = 0: Disable thermal shutdown mode. F0 = 1: Software power-down. F0 = 0: Software power-up.
0	0	0	0	1	0	XX[F13:F0]	Write data in F13 to F0 to OFS0 register.
0	0	0	0	1	1	XX[F13:F0]	Write data in F13 to F0 to OFS1 register.
0	0	0	1	0	0	XX[F13:F0]	Write data in F13 to F0 to OFS2 register.
0	0	0	1	0	1	See Table 18	Select register for readback.
0	0	0	1	1	0	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 0.
0	0	0	1	1	1	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 1.
0	0	1	0	0	0	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 2.
0	0	1	0	0	1	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 3.
0	0	1	0	1	0	XXXX XXXX [F7:F0]	Write data in F7 to F0 to A/B Select Register 4.
0	0	1	0	1	1	XXXX XXXX [F7:F0]	Block write to A/B select registers. F7 to F0 = 0: Write all 0s (all channels use the X2A register). F7 to F0 = 1: Write all 1s (all channels use the X2B register).
0	1	1	1	0	0	Reserved	

Table 18. Address Codes for Data Readback[1]

F15	F14	F13	F12	F11	F10	F9	F8	F7	Register Read
0	0	0	Bit F12 to Bit F7 select the channel to be read back, from Channel 0 = 001000 to Channel 39 = 101111						X1A register
0	0	1							X1B register
0	1	0							C register
0	1	1							M register
1	0	0	0	0	0	0	0	1	Control register
1	0	0	0	0	0	0	1	0	OFS0 data register
1	0	0	0	0	0	0	1	1	OFS1 data register
1	0	0	0	0	0	1	0	0	OFS2 data register
1	0	0	0	0	0	1	1	0	A/B Select Register 0
1	0	0	0	0	0	1	1	1	A/B Select Register 1
1	0	0	0	0	1	0	0	0	A/B Select Register 2
1	0	0	0	0	1	0	0	1	A/B Select Register 3
1	0	0	0	0	1	0	1	0	A/B Select Register 4

[1] Bit F6 to Bit F0 are don't cares for the data readback function.

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Design the PCB on which the AD5371 is mounted so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5371 is in a system where multiple devices require an AGND-to-DGND connection, make the connection at one point only. Establish the star ground point as close as possible to the device. For supplies with multiple pins (V_{SS}, V_{DD}, DV_{CC}), it is recommended that these pins be tied together and that each supply be decoupled only once.

The AD5371 should have ample supply decoupling of 10 µF in parallel with 0.1 µF on each supply, located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI)—typical of the common ceramic types that provide a low impedance path to ground at high frequencies—to handle transient currents due to internal logic switching.

Avoid digital lines running under the device because they can couple noise onto the device. Allow the analog ground plane, however, to run under the AD5371 to avoid noise coupling. The power supply lines of the AD5371 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Shield fast switching digital signals with digital ground to avoid radiating noise to other parts of the board, and never run them near the reference inputs. It is essential to minimize noise on all VREF lines.

Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best approach, but it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

As is the case for all thin packages, care must be taken to avoid flexing the package and to avoid a point load on the surface of this package during the assembly process.

POWER SUPPLY SEQUENCING

When the supplies are connected to the AD5371, it is important that the AGND and DGND pins be connected to the relevant ground plane before the positive or negative supplies are applied. In most applications, this is not an issue because the ground pins for the power supplies are connected to the ground pins of the AD5371 via ground planes. When the AD5371 is to be used in a hot-swap card, care should be taken to ensure that the ground pins are connected to the supply grounds before the positive or negative supplies are connected. This is required to prevent currents from flowing in directions other than toward an analog or digital ground.

INTERFACING EXAMPLES

The SPI interface of the AD5371 is designed to allow the part to be easily connected to industry-standard DSPs and microcontrollers. Figure 24 shows how the AD5371 connects to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5371, as well as programmable input/output pins that can be used to set or read the state of the digital input or output pins associated with the interface.

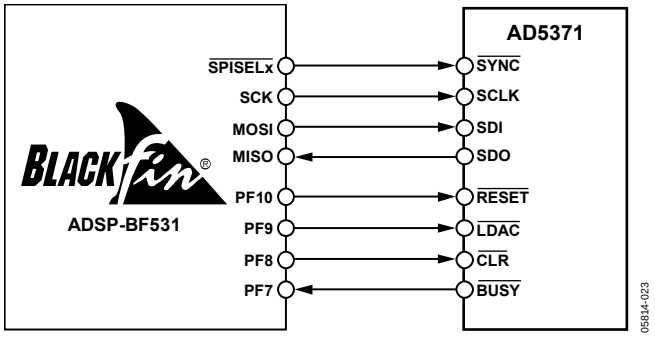


Figure 24. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating-point DSP with two serial ports (SPORTs). Figure 25 shows how one SPORT can be used to control the AD5371. In this example, the transmit frame synchronization (TFSx) pin is connected to the receive frame synchronization (RFSx) pin. Similarly, the transmit and receive clocks (TCLKx and RCLKx) are also connected. The user can write to the AD5371 by writing to the transmit register of the ADSP-21065L. A read operation can be accomplished by first writing to the AD5371 to tell the part that a read operation is required. A second write operation with an NOP instruction causes the data to be read from the AD5371. The DSP receive interrupt can be used to indicate when the read operation is complete.

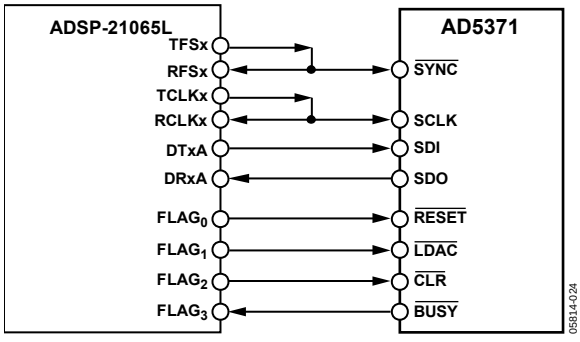
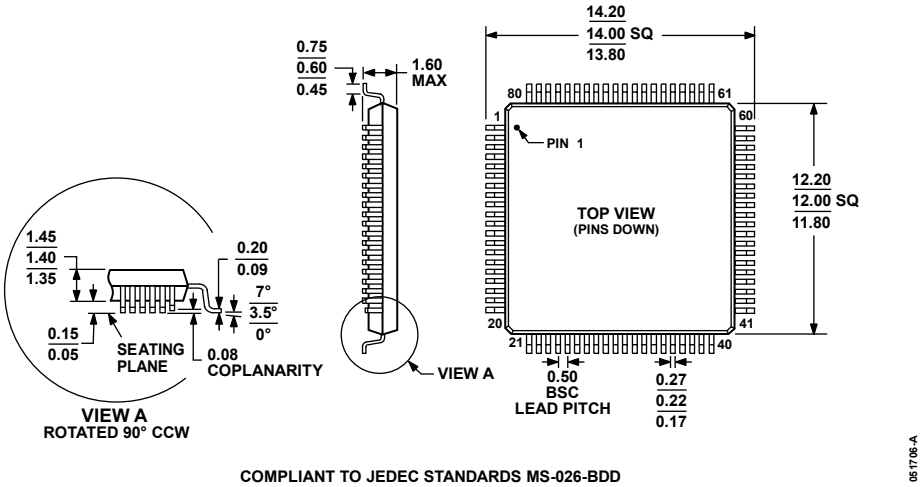


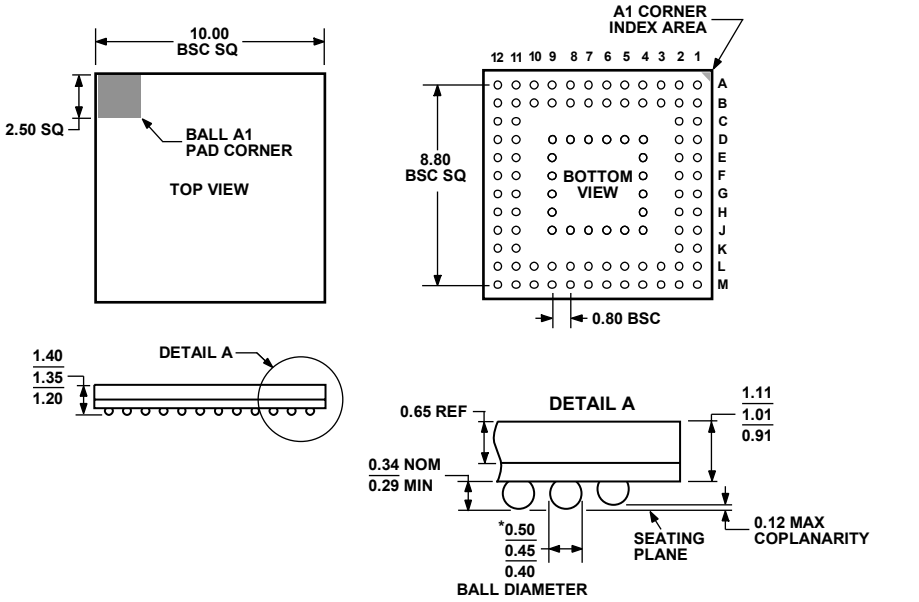
Figure 25. Interfacing to an ADSP-21065L DSP

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BDD

Figure 26. 80-Lead Low Profile Quad Flat Package [LQFP]
ST-80-1
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-205AC
WITH THE EXCEPTION TO BALL DIAMETER.

Figure 27. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD5371BSTZ[1]	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD5371BSTZ-REEL[1]	−40°C to +85°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-1
AD5371BBCZ[1]	−40°C to +85°C	100-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-100-2
AD5371BBCZ-REEL[1]	−40°C to +85°C	100-Ball Chip Scale Package Ball Grid Array (CSP_BGA)	BC-100-2
EVAL-AD5371EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

D05814-0-3/08(B)